Please add the following new claim.

--22. (New) The apparatus of claim 14, having a first level of transistors and a second level of transistors in the Z-dimension.--

REMARKS

Claims 1-13 were cancelled and new claims 14-21 were added in a Preliminary Amendment mailed on October 7, 1999. Claims 14-21 have been examined and claims 14, and 17-21 remain in the Application. The United States Patent and Trademark Office ("USPTO") rejects claims 15 and 16 under 35 U.S.C. § 112, second paragraph. Claims 20-21 are rejected under 35 U.S.C. § 112. Claims 14-21 are rejected under 35 U.S.C. § 103(a).

A. Title

Applicant respectfully asserts that the title "Method for Delaminating A Thin Film Using Non-Thermal Techniques" is sufficiently descriptive because the title includes "delaminating a thin film" which is a feature of one of the techniques described in the patent application. Moreover, the Manual of Patent Examining Procedure, Section 609 and 40 C.F.R. §§ 606 and 606.01, require that the title be brief. Adding words to the title may violate this requirement. Applicant respectfully asserts that the title should remain unchanged.

B. 35 U.S.C. § 112: Rejection of Claims 15-16

The USPTO rejects claims 15-16 under 35 U.S.C. § 112, second paragraph, as indefinite because of the phrase "damaged surface." Applicant has cancelled claims 15 and 16. The rejection to claims 15 and 16 under 35 U.S.C. § 112, second paragraph, should be withdrawn since claims 15 and 16 have been cancelled. Applicant has

amended claim 14 to include damaged surface. Applicant provides the following explanation of damaged surface. Damaged surface 304, referred to on p. 8, line 19 of the Application, is due to the implantation of hydrogen. The high implant dose of hydrogen causes embrittlement of the silicon crystal lattice. During heating to 400°C, the implanted hydrogen in the semiconductor film diffuses into the embrittled region causing pressure to build up and the semiconductor film to delaminate.

Damaged surface 304 is used in the process of making an integrated circuit. Damage surface 304 weakens existing bonds between the semiconductor film and the first substrate. Application, p. 8, lines 18-20. Applicant respectfully asserts that the explanation of "damaged surface" addresses the concern raised by the USPTO.

C. **35 U.S.C. § 102(e): Rejection of Claims 20-21**

The USPTO rejects claims 20-21 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,744,866, issued to Horiba ("*Horiba*"). Claim 20 relates to an apparatus comprising a substrate that has a first oxide film formed thereon. A metal film is formed on the first oxide film. The first oxide film debonds the metal film from the substrate. A second oxide layer is formed on the metal film. A semiconductor film is formed on the second oxide film in which the semiconductor film has at least one active device formed therein. *Horiba* relates to low resistance ground wiring in a semiconductor device. More specifically, *Horiba* relates to fabricating a semiconductor device that includes:

> "There is further provided a semiconductor device including (a) a semiconductor substrate, (b) a first insulating film formed partially on the semiconductor substrate, (c) gate electrodes formed on the first insulating film, the gate

> electrodes having a two-layered structure including a first conductive film and a second insulating film lying over the first conductive film, (d) a diffusion layer formed at a surface of the semiconductor substrate around the gate electrodes, (e) an insulating sidewall film formed around a sidewall of the gate electrodes, (f) a third insulating film partially covering the semiconductor substrate, the insulating sidewall film and the gate electrodes so that the diffusion layer, a part of the gate electrodes and a top edge of the insulating sidewall film are in exposure, (g) a second conductive film covering the third insulating film, exposed part of the gate electrodes, exposed top edge of the insulating sidewall film and the semiconductor substrate, (h) a third conductive film covering the second conductive film, (i) a fourth insulating film having a planarized top surface at such a level that a top surface of the third conductive film is in exposure, and (j) a fourth conductive film bridging over the top surface of the third conductive film. The fourth conductive film, the fourth insulating film, the third conductive film and the second conductive film cooperate with one another to form a ground wiring layer.

Horiba, col. 4, lines 14-38. *Horiba* fails to disclose a "first oxide film [that] debonds the metal film from the substrate" as in the claimed invention. Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) to claim 20. Since claim 21 depends from claim 20, claim 21 has at least the limitations of claim 20. Claim 21, therefore, is also not anticipated by *Horiba* for at least the reasons that claim 20 is not anticipated by *Horiba*.

For the above-stated reasons, Applicant asserts that claims 20-21 are not anticipated by the *Horiba*. Applicant respectfully requests that the Examiner withdraw the rejection to claims 20-21 under 35 U.S.C. § 102(b).

D. <u>35 U.S.C. § 103(a): Rejection of Claims 14-21</u>

The Examiner rejects claims 14-21 under 35 U.S.C. § 103(a) as unpatentable based upon *Horiba*. Claim 14 relates to an apparatus comprising a first substrate with a semiconductor film formed thereon wherein the semiconductor film is demarcated from the rest of the first substrate by a damaged surface with the

damaged surface being removed. A second substrate has a metal film formed thereon. The second substrate is bonded to the second film of the first substrate.

Horiba fails to teach or suggest all of the elements of claim 14. For example, *Horiba* fails to teach or suggest the use of a damaged surface that is subsequently removed. See claim 1, lines 3-4. If the Examiner believes that *Horiba* teaches this feature, Applicant requests that the Examiner provide a citation to support such an assertion.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 4/10/00

By: _____
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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited as First Class Mail with the United States Postal Service in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on 4/10/00.

Nadya Gordon 4/10/00
Nadya Gordon *Date*